## REMARKS

### Present Status of the Application

The Office Action mailed April 21, 2003 rejected all presently pending claims 1-16 and 18-21. Specifically, claims 1-16 and 18-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 6,118,154) in view of Hu el al. (US 6,121,077), Erdeljac et al. (US 5,554,873) and Japanese Patent #4-76959. In response thereto, Applicants have deleted claim 18 and amended claims 1, 9, 14, 15, 19 and 21. Reconsideration of claims 1-16 and 19-21 is respectfully requested.

### Summary of the Application

The present invention is directed to an ESD protection structure electrically connected between an input pad and a node which an internal circuit is electrically connected to. The ESD protection structure comprises an input resistor electrically coupled between the input pad and the node, and a single crystal silicon-sided junction diode electrically coupled between one terminal of a corresponding power supply and the node. The input resistor includes a plurality of single crystal Si resistors formed over an insulating material layer and coupled between the input pad and the node.

**Discussion of Office Action Rejections**

Applicants respectfully point out that there is a contradiction in the Office Action. As stated in Page 3: "*Yamaguchi et al. teach in the embodiment of figure 10 a junction diode without a control gate electrode*", while in Page 4: "*Yamaguchi et al. teach in figure 10 an input resistor comprising a plurality of single resistors 64 formed over the insulating material layer, wherein each of the resistors is electrically coupled between the input pad and the node*". Apparently, the structure illustrated in FIG. 10 ***cannot be simultaneously a junction diode and an input resistor***, as shown in FIG. 4 of Yamaguchi et al., since the junction diode 38/39 and the input resistor 36/37 are totally different components in the ESD protection structure,

More specifically, according to the descriptions (col. 11, lines 13-16) related to FIG. 10 in Embodiment 4: "*Thus, $p^-$-type region 64 and a plurality of $n^+$-type regions 61 form diode 38 in FIG. 4, and a plurality of $p^+$-type regions 62 and $n^-$-type region 63 form diode 39 in FIG. 4.*", **the structure illustrated in FIG. 10 is actually a junction diode coupled between a power supply and the node, but not an input resistor coupled between the input pad and the node.** Meanwhile, each $p^-$-type region (single resistor) 64 is a part of the junction diode 38 in FIG. 4, ***but not a part of the input resistor 36/37***. Therefore, each $p^-$-type region (single resistor) 64 is coupled between the power supply and the node, ***but not between the input pad and the node.***

In other words, ***Yamaguchi et al. fail to teach or suggest the input resistor of this invention that comprises a plurality of single resistors formed over an insulating material layer and electrically coupled between the input pad and the node.*** FIG. 10 of Yamaguchi et al. does teach a junction diode that comprises a plurality of single diodes electrically coupled

between the power supply and the node.

Moreover, Applicants have confirmed that the other three cited Patents, Hu el al., Erdeljac et al. and Japanese Patent #4-76959, also fail to teach or suggest the feature, i.e., an input resistor comprising a plurality of single resistors formed over an insulating material layer and electrically coupled between the input pad and the node. Therefore, ***the feature cannot be obtained from the combination of the four cited Patents.***

***However, the said feature is disclosed in original independent claim 9 and amended independent claims 1, 14 and 21 of this invention*** as follows, marked with underlines, and is supported by FIG. 3 of this invention:

1. (Currently Amended) An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit, ..... the ESD protection structure comprising:
an input resistor including a plurality of single crystal Si resistors formed over an insulating material layer, electrically coupled between the input pad and the node; and
at least a single crystal silicon-sided junction diode ..... .

9. (Currently Amended) An ESD protection structure ..... comprising:
an input resistor including a plurality of single resistors formed over the insulating material layer, wherein each of the single resistors is electrically coupled between the input pad and the node; and
at least a single crystal sided junction diode ..... .

14. (Currently Amended) A semiconductor structure of ESD protection, ..... comprising:
.....;
an input resistor including a plurality of single crystal Si resistors, formed over the insulating layer;
at least a single crystal Si-sided junction diode formed over the insulating layer;
..... .

21. (Currently Amended) An ESD protection structure ..... comprising:
an input resistor including a plurality of single crystal Si resistors formed on an insulating material layer, electrically coupled between the input pad and the node; and
a single crystal layer formed over the insulating material layer ..... .
***(Emphases added)***

For at least the reasons mentioned above, Applicants respectfully submit that independent claims 1, 9, 14 and 21 patently define over the prior art.

For at least the same reasons mentioned above, Applicants respectfully submit that claims 2-8 dependent from claim 1, claims 10-13 from claim 9, claims 15-16 and 19-20 from claim 14 also patently define over the prior art.

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## CONCLUSION

For at least the forgoing reasons, it is believed that all pending claims 1-16 and 19-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809